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RESEARCH ARTICLE

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Flexible organic integrated circuits free of parasitic capacitance fabricated through a simple dual self-alignment method

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Abstract

In integrated circuits (ICs), the parasitic capacitance is one of the crucial factors that degrade the circuit dynamic performance; for instance, it reduces the operating frequency of the circuit. Eliminating the parasitic capacitance in organic transistors is notoriously challenging due to the inherent tradeoff between manufacturing costs and interlayer alignment accuracy. Here, we overcome such a limitation using a cost-effective method for fabricating organic thin-film transistors and rectifying diodes without redundant electrode overlaps. This is achieved by placing all electrodes horizontally and introducing sub-100 nm gaps for separation. A representative small-scale IC consisting of five-stage ring oscillators based on the obtained nonparasitic transistors and diodes is fabricated on flexible substrates, which performs reliably at a low driving voltage of 1 V. Notably, the oscillator exhibits signal propagation delays of 5.8 μs per stage at a supply voltage of 20 V when utilizing pentacene as the active layer. Since parasitic capacitance has been a common challenge for all types of thin-film transistors, our approach may pave the way toward the realization of flexible and large-area ICs based on other emerging and highly performing semiconductors.

KEYWORDS
flexible electronics, integrated circuits, organic thin-film transistors, parasitic capacitance, self-alignment

1 | INTRODUCTION

Organic integrated circuits (ICs) have attracted significant research interest due to the unique advantages of organic thin-film transistors (OTFTs) as their fundamental building blocks, including low-cost manufacturing, mechanical flexibility, and facile processability for large-area fabrication.[1,2] OTFTs serve as the key switching element in logic circuits and have witnessed an impressive improvement in their quasistatic characteristics over the past few decades. For instance, the charge-carrier mobility (μ) of OTFTs has been reported to exceed 30 and 10 $cm^2/(V{\cdot}s)$ for small-molecule semiconductors[3–5] and semiconducting polymers,[6–9] respectively. These achievements can be attributed to the synergistic optimization of the molecular structure, material morphology, key interfaces, and device configuration[10–14]; most of these optimizations aim to maximize the mobility of discrete devices. However, when transistors are integrated into practical circuits and subjected to continuous ON and OFF switching, the presence of the parasitic capacitance (C_p) becomes a critical factor that needs to be considered. Optimizing C_p is essential as its charging and discharging processes can significantly reduce the operating speed of the circuit. Moreover, the alternating current (AC) passing through C_p can lead to increased heat generation and reduced energy efficiency when the circuit is operating at high frequencies. The existence of C_p has thus emerged as one of the major limitations preventing OTFTs from serving as the foundation of GHz flexible electronics.[15,16]

Efforts aimed at reducing or eliminating C_p in OTFTs necessitate the design of a feasible device configuration with minimized lateral overlap between the gate (G) electrode and source (S)/drain (D) electrodes as well as the exploration of cost-effective manufacturing methods.[17–20] This endeavor should be considered a priority within the field. The rationale behind this urgency lies in the fact that the mobility of a specific organic semiconductor (OSC) is not constant but rather highly sensitive to various factors, including the channel length, contact resistance, dielectric surface modification, and fabrication process.[21] Therefore, it is expected that the mobility of OSCs relies heavily on the device configuration and fabrication process adopted for achieving a C_p reduction. In other words, the further improvement in the charge-carrier mobility of OSCs can lead to higher-performance flexible ICs only when achieved through a viable C_p-free transistor configuration.

Notably, the adoption of OSCs as the active layer in ICs offers unique advantages, such as low-cost manufacturing and potential application to large-area and flexible occasions.[22] So, these prerequisites have limited the choice of patterning techniques in organic electronics. For example, techniques involving heavy instrumentation, such as deep ultraviolet lithography and electron-beam lithography, should be immediately excluded.[23,24] Additionally, due to the inevitable deformation that occurs when manufacturing on flexible substrates, it seems unattainable to simultaneously achieve large-area patterning and high-precision alignment by simply using hard masks in sequence. The self-alignment technology, which utilizes the edge of a pattern layer to physically define another layer, represents a feasible approach to overcome these challenges, and as such, has garnered increasing interest within the field of organic electronics.[25] Notably, self-alignment techniques have been found to be capable of fabricating nanoelectrodes with a high accuracy in single transistors.[18,19,26–28] Nevertheless, to the best of our knowledge, the realization of self-aligned organic ICs has rarely been achieved.[29]

Here, we propose an ideal configuration for OTFTs free of C_p by horizontally arranging the S, G, and D electrodes with sub-100 nm gaps.[17] More importantly, this highly precise device structure can be conveniently realized through a cost-effective one-step photolithographic exposure process. By employing a "dual self-alignment" (d-SA) technique combining wet-etching and lift-off processes, the gaps between the S/D electrodes and the G electrode can be controlled to be well below 100 nm, thereby completely avoiding their overlap while maintaining a low charge-carrier injection barrier. After thorough optimization, the prepared OTFTs based on pentacene exhibit excellent performance in this configuration, with mobilities exceeding 0.4 $cm^2/(V{\cdot}s)$ and ON/OFF current ratios surpassing 10^5. Furthermore, we demonstrate the compatibility of the d-SA technology with large-area flexible substrates by fabricating small-scale ICs, including five-stage ring oscillators (ROs) and an OTFT array with 100 transistors on a 3 cm × 3 cm polyethylene terephthalate (PET) sheet. These results validate the practical applicability of the d-SA technology in the manufacturing of ICs, particularly on flexible substrates.

2 | RESULTS AND DISCUSSION

2.1 | Fabrication of C_p-free OTFTs through the d-SA technique

In OTFTs, the electrical capacitor formed between the semiconducting channel and the G electrode is commonly referred to as the active capacitance (C_a) as it plays a crucial role in the G-modulated transconductance

through the charging and discharging processes.[30] However, the overlap region between the S/D electrodes and the G electrode introduces an undesired charge reservoir, known as C_p, which ideally should be minimized in the transistor (Figure 1A). The basic strategy to completely remove C_p from OTFTs is to precisely align the G electrode and the S/D electrodes, thereby preventing these regions from overlapping

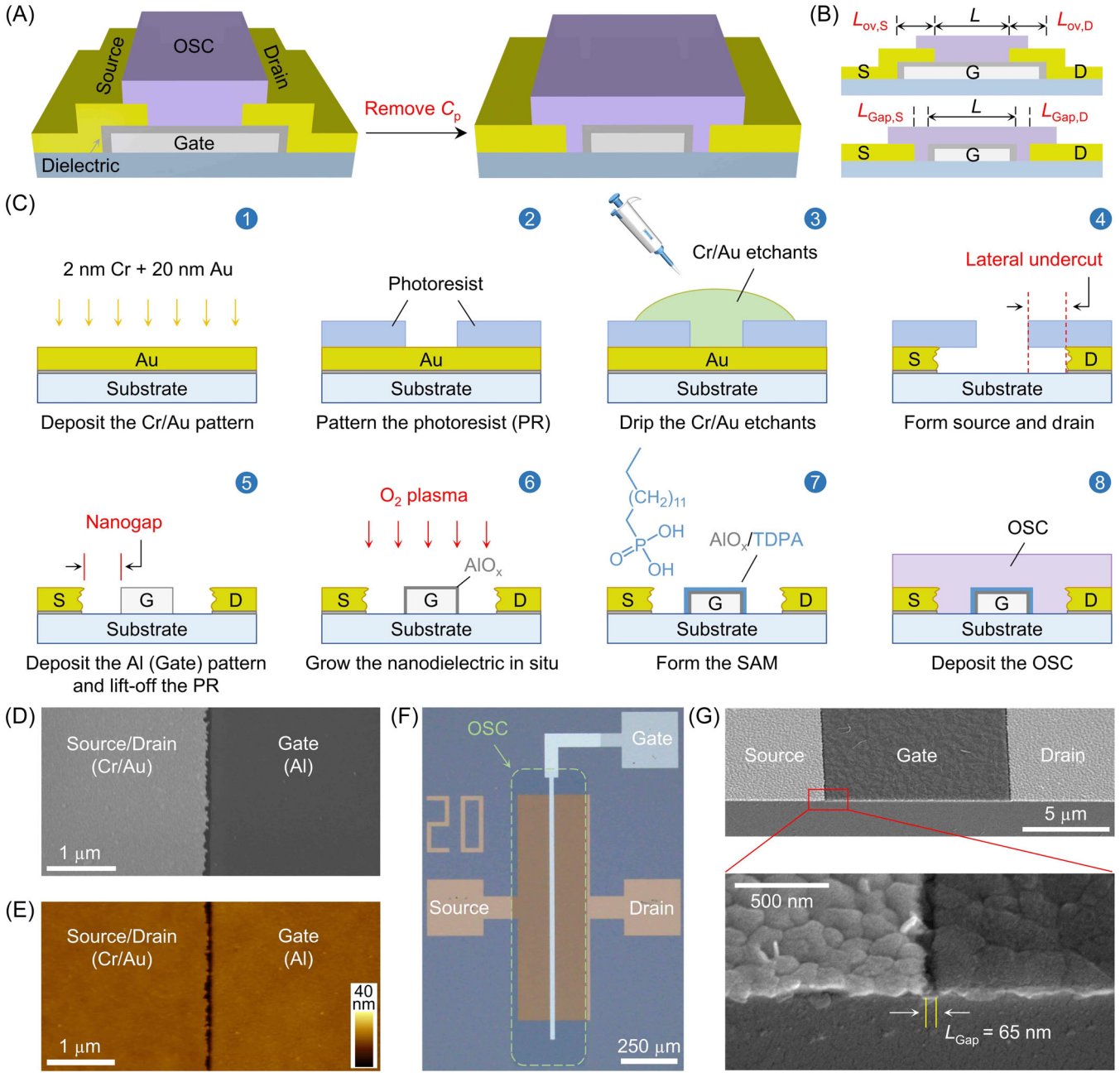

FIGURE 1 Fabrication and structural characterization of a C_p-free organic thin-film transistor (OTFT). (A, B) Schematic and corresponding cross section of a typical OTFT with C_p originating from the lateral overlap (L_{ov}) between the G/S and G/D electrodes (left of (A) and top of (B), respectively) and a C_p-free OTFT fabricated using the d-SA technique (right of (A) and bottom of (B), respectively). (C) Schematic depicting the d-SA technique. The geometric parameters of the obtained nanostructure can be tuned by changing various factors, such as the etching time, etchant concentration, and etching temperature. (D, E) Scanning electron microscope (SEM) (D) and atomic force microscopy (AFM) (E) images illustrating the uniformity and length of the nanogap (L_{Gap}) separating the D/S (Cr/Au, left) and G (Al, right) electrodes in a coplanar OTFT. (F) Photography of a C_p-free OTFT with a channel length (L) of 20 μm. (G) SEM image (top) of a cross-sectional device based on pentacene with a substrate tilt angle of 45° and magnified view (bottom) of the area marked in red with the same tilt angle.

(Figure 1B). As a significant step forward compared with previously reported self-alignment procedures, in this work, C_p-free OTFTs are fabricated via the d-SA technique, which is depicted in Figure 1C and described in detail in the Experimental Section of Supporting Information S1. This technique involves (i) the patterning of a photoresist (PR) layer through a one-step photolithographic exposure to define the Au/Cr S and D electrodes using wet etching and (ii) the formation of the Al G electrode using the lift-off process. The gap between the Au/Cr and Al electrodes can be tailored by carefully tuning the parameters of the wet-etching process.

Al was selected as the G electrode due to its ability to facilitate the conformal growth of an ultrathin AlO_x dielectric layer through oxidization.[31] The in situ formation of a nanometer-thick oxide layer not only reduces the operating voltage to below 5 V,[32] which is beneficial for minimizing the power consumption of ICs and ensuring the safety of wearable organic electronics, but also improves the quality of the interface between the AlO_x dielectric layer and the OSC by modifying the surface of AlO_x with alkyl phosphonic acid (PA) self-assembled monolayer (SAM).[33,34] The nanogap between the G electrode and the S/D electrodes is achieved via the lateral undercut that is realized during the wet-etching process (the 4th step in Figure 1C),[35] and its length can be easily tuned from 600 to 65 nm by changing the etching conditions, such as the etching time and etchant concentration (Supporting Information S1: Figure S1). The morphology of the fabricated S, G, and D electrodes of the C_p-free OTFT was characterized using scanning electron microscopy (SEM) and atomic force microscopy (AFM), as shown in Figure 1D,E and Supporting Information S1: Figure S2.

To enable the preparation of ICs, vacuum-evaporated OSCs were chosen for fabricating the C_p-free OTFTs, with their channel length ranging systematically from 2 to 20 μm, as shown in Figure 1F and Supporting Information S1: Figure S3. Notably, the thicknesses of the G electrode and the S/D electrodes could be made to match with a high degree of accuracy (Figure 1E and Supporting Information S1: Figure S2B), resulting in a coplanar structure that holds potential for the future lamination of semiconducting organic single crystals with a flat surface.[36–38] It is worth emphasizing that our d-SA technique exhibits an alignment accuracy well below 100 nm. However, a moderate nanogap width of 65 nm was found to be suitable for reducing the contact resistance while ensuring an acceptable device yield for the successful fabrication of small-scale integrated circuits (SSICs) (Figure 1G). We explored a range of devices with different G-to-contact nanogap lengths (L_{Gap}) to investigate the impact of different L_{Gap} values on the performance of the OTFTs.

2.2 | Characterization and optimization of the C_p-free OTFTs

Figure 2A illustrates a typical transfer characteristic of a C_p-free pentacene-based TFT, where the nanogap between the S/D electrodes and the G electrode is controlled to be approximately 65 nm. The transfer curve exhibits a negligible hysteresis, suggesting the formation of a high-quality interface between the dielectric and the semiconductor after the SAM modification. Moreover, the G leakage current (I_G) remains below 1 nA under a 3 V operating voltage, demonstrating the excellent dielectric properties of the hybrid AlO_x/SAM layer. Its specific capacitance was measured to be 710 nF/cm^2 (Supporting Information S1: Figure S4), which is consistent with previous reports.[34,39] The mobility extracted from the saturation region in Figure 2A is 0.27 cm^2/(V·s). However, the output curve shows clear nonideal characteristics, such as a slightly "S-shaped" current depression in the linear region and a poor current saturation in the saturation region (Figure 2B). These observations suggest the need for further optimization of contact resistance.

To address the issue of contact resistance, we fabricated devices with systematically varied L_{Gap} and measured their mobilities (Figure 2C). As expected, the charge-carrier mobility decreases by 78.9% (from 0.27 to 0.057 cm^2/(V·s)) as L_{Gap} increases from 65 to 550 nm (Supporting Information S1: Figure S5). This decrease can be attributed to the additional electrical resistance introduced by the longer L_{Gap} in OTFTs, which hinders the injection of charge carriers into the conducting channel and negatively impacts the device performance.[40] It is reasonably inferred that this extra resistance is the resistance of the OSCs within the nanogap, which is taken into account by the total contact resistance. However, reducing the nanogap further to match the thickness of the Au electrodes (20–30 nm) poses challenges to the wet-etching process of Au, which can reduce the device yield. Therefore, it is necessary to explore alternative strategies for enhancing the conductivity of OSCs within the nanogap that do not require further nanogap reduction.

Fortunately, it was found that the contact resistance could be effectively reduced without introducing additional fabrication steps. The 2-nm-thick Cr layer used as an adhesion layer for the Au electrode was also found to be capable of serving as an efficient hole dopant for *p*-type OSCs, such as pentacene and copper phthalocyanine

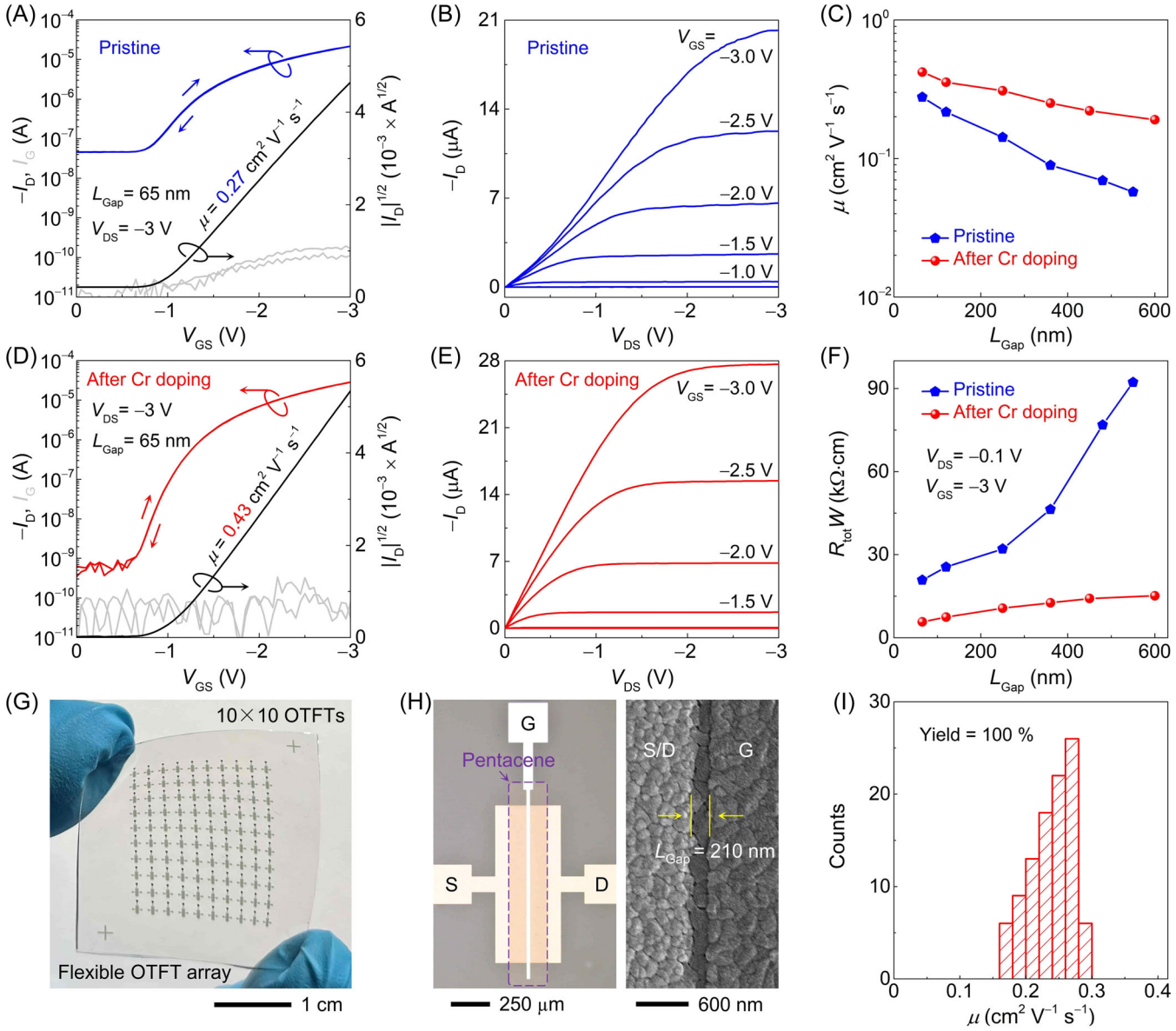

FIGURE 2 Electrical characteristics of pentacene-based C_p-free organic thin-film transistors (OTFTs). (A–F) Transfer (A, D) and output (B, E) curves of the C_p-free OTFTs with a channel length/width of 20/1000 μm based on pentacene grown on a 65-nm-long nanogap before (A, B) and after (D, E) Cr doping. Plots of (C) the mobility and (F) the total contact resistance (R_{tot}) as a function of the nanogap length (L_{Gap}). (G) Photograph of a pentacene-based C_p-free OTFT array fabricated on a flexible, transparent PET substrate (3 cm × 3 cm). (H) Optical image of an individual OTFT from (G) with a channel length/width of 20/1000 μm (left) and corresponding SEM image of the channel region indicating a G-to-contact nanogap of 210 nm (right). (I) Distribution of the device mobilities.

(CuPc). Consequently, the electrical conductivity of OSCs in the contact regions could be enhanced through doping.[41] It is worth noting that the nanometer-thick Cr layer tends to undergo oxidation during the evaporation process, especially when stored in air or subjected to an oxygen plasma treatment. Indeed, it was found that after the complete removal of the Au layer within the nanogaps using an I_2/KI etchant, the remaining Cr layer had already been oxidized to CrO_x. This metal oxide is commonly used in the doping of OSCs alongside other metal oxides, such as MoO_x, Mn_3O_4, and V_2O_5.[42–45] The transition of Cr from a metallic state to an oxide state was also confirmed by the fact that the Cr layer was not electrically conducting (Supporting Information S1: Figure S6).

To investigate the effect of the doping of the OSCs with oxidized Cr, we measured the sheet conductivity of the pentacene and CuPc films by fabricating two-terminal devices. As shown in Supporting Information S1: Figure S6, the pentacene film deposited on naked CrO_x

exhibited a huge increase in conductivity, nearly four orders of magnitude higher than that of the pentacene film grown on a pristine SiO_2 substrate. During the fabrication of the C_p-free OTFTs, the devices and substrate were immersed in an *n*-tetradecyl phosphonic acid (TDPA) solution to modify the AlO_x nanodielectric layer. Such a processing step inevitably resulted in the formation of an adhesion layer composed of TDPA-molecules on CrO_x, as confirmed by AFM (Supporting Information S1: Figure S7), since PA and its phosphonate ester derivatives can form covalently bonded PA-SAMs on a broad range of inorganic oxides.[46] While the presence of TDPA molecules adhering to the CrO_x surface mitigates slightly the effect of CrO_x doping compared with the bare surface of CrO_x, the conductivities of both the pentacene and CuPc films remain significantly higher than that observed on bare SiO_2 without doping.

The spontaneous oxidation of the nanometer-thick Cr layer ensures that it does not cause a short circuit by electrically connecting the S/D electrodes and the G electrode. Instead, it provides an opportunity to optimize the contact resistance through doping. Therefore, we decided to preserve the Cr adhesion layer by saving the Cr wet-etching step in the manufacturing process (Supporting Information S1: Figure S8). Unsurprisingly, the hole mobility of the pentacene-based OTFT increases significantly by 59% from 0.27 (Figure 2C) to 0.43 $cm^2/(V{\cdot}s)$ simply by retaining the Cr layer in the nanogap (L_{Gap}: 65 nm; $L_{channel}$: 20 μm). The ON/OFF current ratio of the transistor also exhibits a notable improvement from 10^3 to 10^5 (Figure 2D). More importantly, the zone-selective doping in nanogaps reduces the sensitivity of the performance of the C_p-free OTFTs to variations in the nanogap length because transistors with a larger L_{Gap} benefit more from CrO_x doping (Figure 2C and Supporting Information S1: Figure S5). This phenomenon brings advantages to the implementation of ICs on large-area substrates by improving the reproducibility of the performance across different devices, especially considering the potential variations in the wet etching of Au.

To gain further insights into the contact resistance, we conducted an analysis of the linear regime of the output curves of the C_p-free OTFTs with different nanogap lengths ranging from 65 to 600 nm (Supporting Information S1: Figure S5). According to Ohm's law, the total device resistance can be determined by measuring D current (I_D) at a small D-S voltage (V_{DS}) while applying a significantly larger G-S voltage (V_{GS}) bias to the transistor to ensure that it operates in the linear regime. Under these conditions, the resistance of the channel region, which is actually a function of V_{GS}, can be considered as a constant part of the total resistance (R_{tot}). As a result, the variation in R_{tot} is primarily influenced by the contact resistance (R_{con}). From Figure 2F, it is evident that for all devices, R_{tot} (and consequently also R_{con}) can be improved through either Cr doping or nanogap shrinkage. In agreement with the mobility results presented in Figure 2C, the extent to which R_{con} can be optimized through Cr doping is considerably greater in devices with relatively large nanogaps (Figure 2F).

Since the morphology of pentacene remains unchanged for all nanogap widths (Supporting Information S1: Figure S9), its intrinsic mobility should remain the same. Therefore, the pronounced performance enhancement can be exclusively attributed to the reduction in R_{con} achieved through the zone-selective doping of the gap region. This hypothesis is supported by the output curves, which exhibit a much better saturation behavior after contact doping, eliminating the previously observed S-shape in the I_D at a low V_{DS} (Figure 2B,E). C_p-free OTFTs with an optimized R_{con} were fabricated using both pentacene and CuPc, with channel lengths ranging from 2 to 20 μm. All devices exhibited distinct field-effect characteristics (Supporting Information S1: Figure S10), and their key parameters are summarized in Supporting Information S1: Table S1. It is worth noting that for both pentacene and CuPc, OTFTs with a channel length of 2 μm showed a lower mobility, approximately one-quarter of that observed in OTFTs with a channel length of 20 μm, which is a common phenomenon in bottom-contact OTFTs.

The reproducibility of the fabrication process is a critical factor for the successful preparation of ICs. To assess this, we characterized 100 pentacene-based OTFTs fabricated in 10 different batches, and their transfer curves are summarized in Supporting Information S1: Figure S11 alongside their mobility and threshold voltage distributions plotted as histograms. In addition, to demonstrate the operational stability of the prepared pentacene-based C_p-free OTFTs doped with Cr in practical applications, we carried out several tests including 2000 ON/OFF switching cycles, a 1-h-long G-bias stress test and 50 times scanning tests (Supporting Information S1: Figure S12). The results of these tests showcase the robustness and reliability of the devices. Furthermore, it is noteworthy that the C_p-free OTFTs are actually recyclable. Specifically, the OSC can be washed away and replaced with another type of semiconductor, as shown in Supporting Information S1: Figure S13. Furthermore, we demonstrated that the semiconductor in the transistors can be changed from CuPc to pentacene as desired. The device can be recycled four times, and retains almost the original performance using the same OSC (Supporting Information S1: Figure S14). This advantage makes C_p-free OTFTs an attractive test platform for diverse semiconductor materials.

The d-SA technology is highly suitable for manufacturing transistors on large-area and flexible substrates, as demonstrated by the fabrication of a 10×10 C_p-free OTFT array on a PET sheet (Figure 2G). To guarantee a 100% device yield on such a large-area substrate, the nanogap was increased to 210 nm by tuning the Au wet-etching process (Figure 2H). All 100 devices exhibit standard transfer and output curves, as shown in Supporting Information S1: Figure S15. The OTFT mobilities are mainly distributed in the range of 0.16–0.30 $cm^2/(V \cdot s)$, with an average value of 0.24 $cm^2/(V \cdot s)$ (Figure 2I). The ON/OFF current ratios of these transistors exceed 10^5. The performance of the OTFT array serves as a crucial benchmark for evaluating the feasibility of the manufacturing process. The high device yield and narrow performance distribution of the array indicate that the d-SA technology is indeed suitable for achieving an extremely high fabrication accuracy through a very simple process.

2.3 | Fabrication and characterization of organic inverters

Inverters are a fundamental component of digital ICs that can be realized using three different strategies: complementary, complementary-like, or unipolar inverters.[47] The former strategy, which involves connecting a pair of *p*-type and *n*-type transistors, results in the realization of what is commonly referred to as a complementary metal-oxide-semiconductor (CMOS) inverter.[48–50] However, as discussed earlier, the role of CrO_x as a hole dopant optimizes the performance of the C_p-free OTFTs, thereby only promoting the utilization of unipolar *p*-type transistors for realizing the so-called PMOS inverters,[51] which merely require pentacene- or CuPc-based transistors. The most commonly used zero-V_{GS}-load logic inverter is here taken as an example[52]; it consists of a driving transistor and a load transistor. In the load transistor, the G and S electrodes are directly connected. Typically, the channel width-to-length ratio (W/L) of the load transistor should be 30 times larger than that of the driving OTFTs. However, this requirement of having a significantly larger load transistor poses unnecessary obstacles for circuit integration and optimization of C_p.

To address the challenge of miniaturizing load transistors, we successfully implemented the d-SA technology to design a novel coplanar rectifying nanodiode, as depicted in Figure 3A. According to the flow chart in Supporting Information S1: Figure S16A, the transistor was converted to an organic load diode by vertically connecting the G and S electrodes in an OTFT. Thanks to the high spatial resolution of the d-SA method, in the load transistors, the channel distance between the S and D electrodes could be finely tuned to be below a few hundreds of nanometers (Figure 3B,C). As shown in Figure 3A,C, the Al electrode covered with AlO_x-SAM was designed to directionally block hole injection from the S electrode because of the electrical field repulsion from Al and the adjacent OSC on Al (Figure 3D). The overall electrical resistance of the rectifying diode could

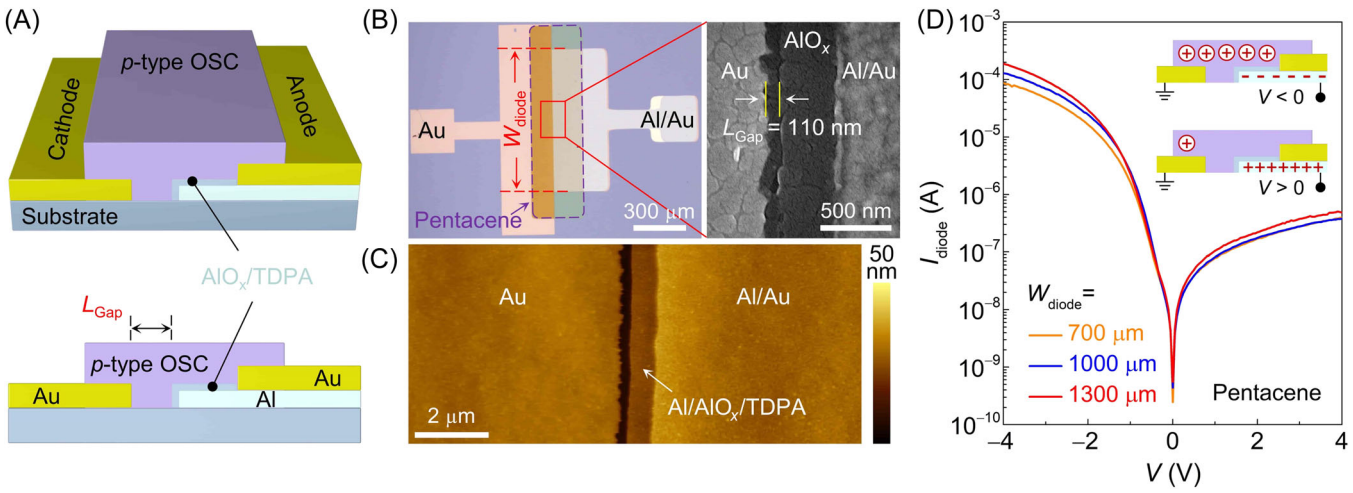

FIGURE 3 Fabrication and characterization of C_p-free organic diodes. (A) Schematic of a C_p-free diode created by merging the G and S electrodes in an organic thin-film transistor (OTFT). (B) Photograph of a diode (left) and scanning electron microscope (SEM) image (right) illustrating the uniformity and width of the nanogap between Au and AlO_x. (C) Atomic force microscopy (AFM) image showing the relative position of the anode and cathode of a diode. (D) Current-voltage (I_{diode}-V) characteristics of pentacene-based C_p-free diodes with different channel widths (W_{diode}) ranging from 700 to 1300 μm. The insets in (D) reveal the working principle of the organic diodes.

be tuned by changing the channel width to match that of the driving OTFTs. Furthermore, the structural parameters of the device could be tailored during the manufacturing process (Supporting Information S1: Figure S16B). The effects of Cr doping and the nanogap length between the D and Al electrodes on the rectifying behavior were thoroughly studied and is summarized in Supporting Information S1: Figure S17. After optimization, the rectification ratio of the pentacene-based coplanar load diode could reach almost 10^3 (Figure 3D).

As depicted in the schematic of Figure 4A and the optical microscopy image of Figure 4B, the PMOS inverter was realized by connecting a C_p-free OTFT with a load rectifying diode. Both components are based on unipolar *p*-type OSCs, such as pentacene and CuPc. To evaluate the performance of the inverters, the output voltage was plotted as a function of the input voltage at a device driving voltage (V_{DD}) of 3 V. The results for the pentacene-based inverters are presented in Figure 4C,D, while Supporting Information S1: Figure S18 displays the results for the CuPc-based inverters. The gain of the inverters remained above 10 when powered by a V_{DD} of 3 V, it decreased slightly to a moderate level of over 5 when a lower driving voltage was used (Figure 4E). Thanks to the remarkable stability and robustness of the pentacene-based C_p-free OTFTs, the resulting inverters can operate even at a low V_{DD} of 1.5 V and show a small hysteresis of less than 0.1 V (Figure 4E). The gain of the obtained PMOS inverters is comparable to that of printed PMOS organic inverters in previous reports for all C_p-free

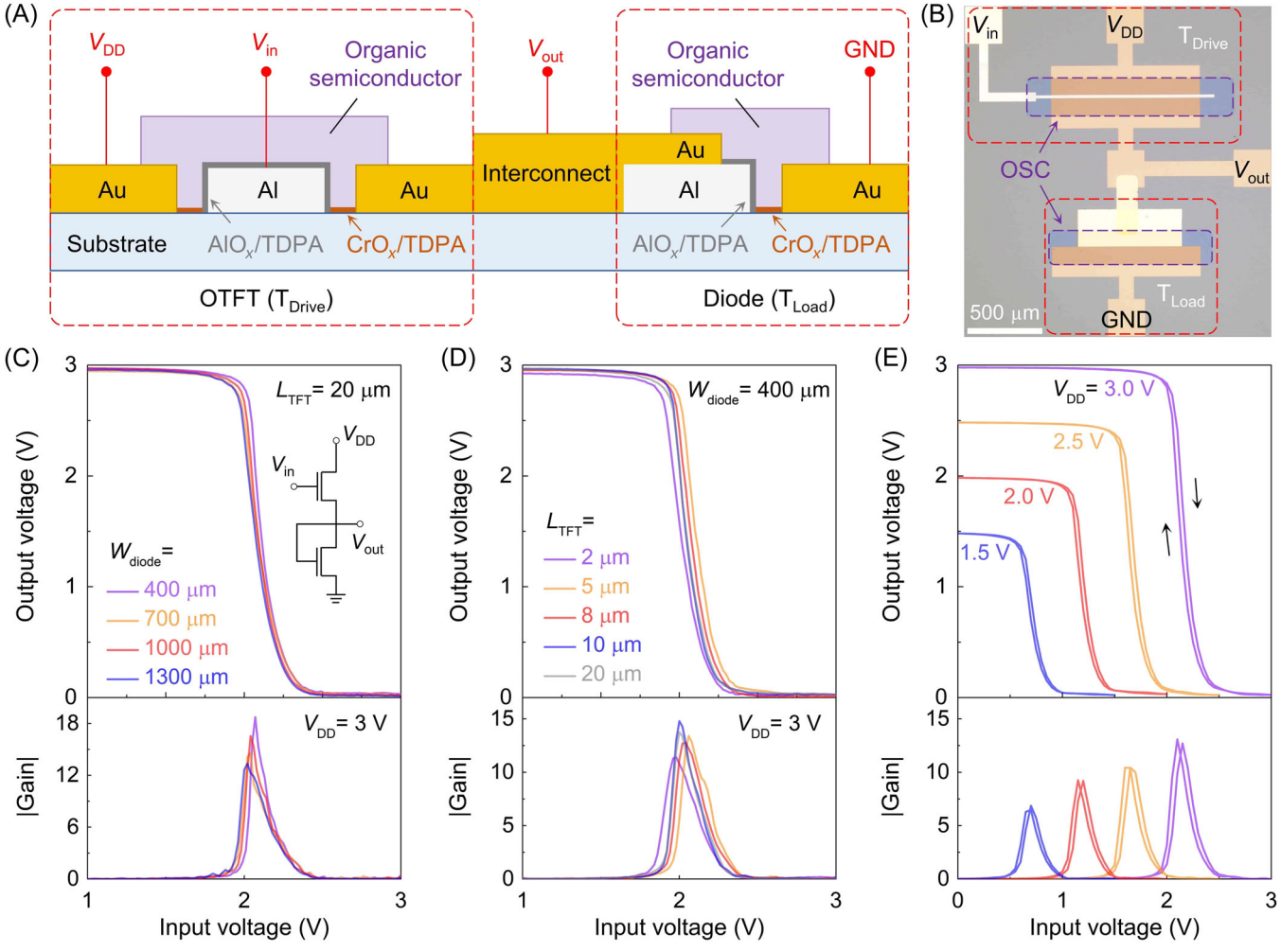

FIGURE 4 Schematic and electrical characteristics of organic inverters made of C_p-free organic thin-film transistors (OTFTs) and diodes. (A) Schematic device structure of an organic inverter consisting of a drive transistor (left, T_{Drive}) and a load diode (right, T_{Load}). (B) Optical image of a pentacene-based inverter. GND represents the ground. (C, D) Output voltage (top) and small-signal gain (bottom) as a function of the input voltage at an operating voltage (V_{DD}) of 3 V. The drive transistors in (C) have a channel length (L_{TFT}) ranging from 2 to 20 μm, and the load diodes in (D) have a channel width (W_{diode}) ranging from 400 to 1300 μm. The inset in (C) shows the circuit diagram of an organic inverter. (E) Electrical characteristics of a pentacene-based inverter made of an OTFT with an L_{TFT} of 20 μm and a diode with a W_{diode} of 400 μm.

OTFTs regardless of the OSC employed and their channel length (Supporting Information S1: Table S2).

2.4 | Dynamic characteristics of five-stage ROs

The RO depicted in Figure 5A is a simple but fully functional SSIC capable of revealing the dynamic properties of the constituent transistors through its oscillation frequencies (f) and propagation delay per stage (τ).[50] To demonstrate the potential of the obtained C_p-free OTFTs and the proposed d-SA technique in realizing organic and flexible ICs, we fabricated a series of PMOS five-stage ROs on both rigid quartz and flexible PET substrates (Figure 5B). These ROs utilize the aforementioned inverters composed of coplanar load diodes and p-type OTFTs, based on either pentacene or CuPc as the OSC, with a channel length (L_{TFT}) ranging from 2 to 20 μm. The SEM images of the nanogap regions in these C_p-free OTFTs are presented in Figure 5C. Interestingly, the etching degree and thus the length of the resulting nanogaps exhibit slight variations depending on L_{TFT} under identical wet-etching conditions (Supporting Information S1: Figure S19). In Figure 5D, the typical output signals of the ROs are plotted to study

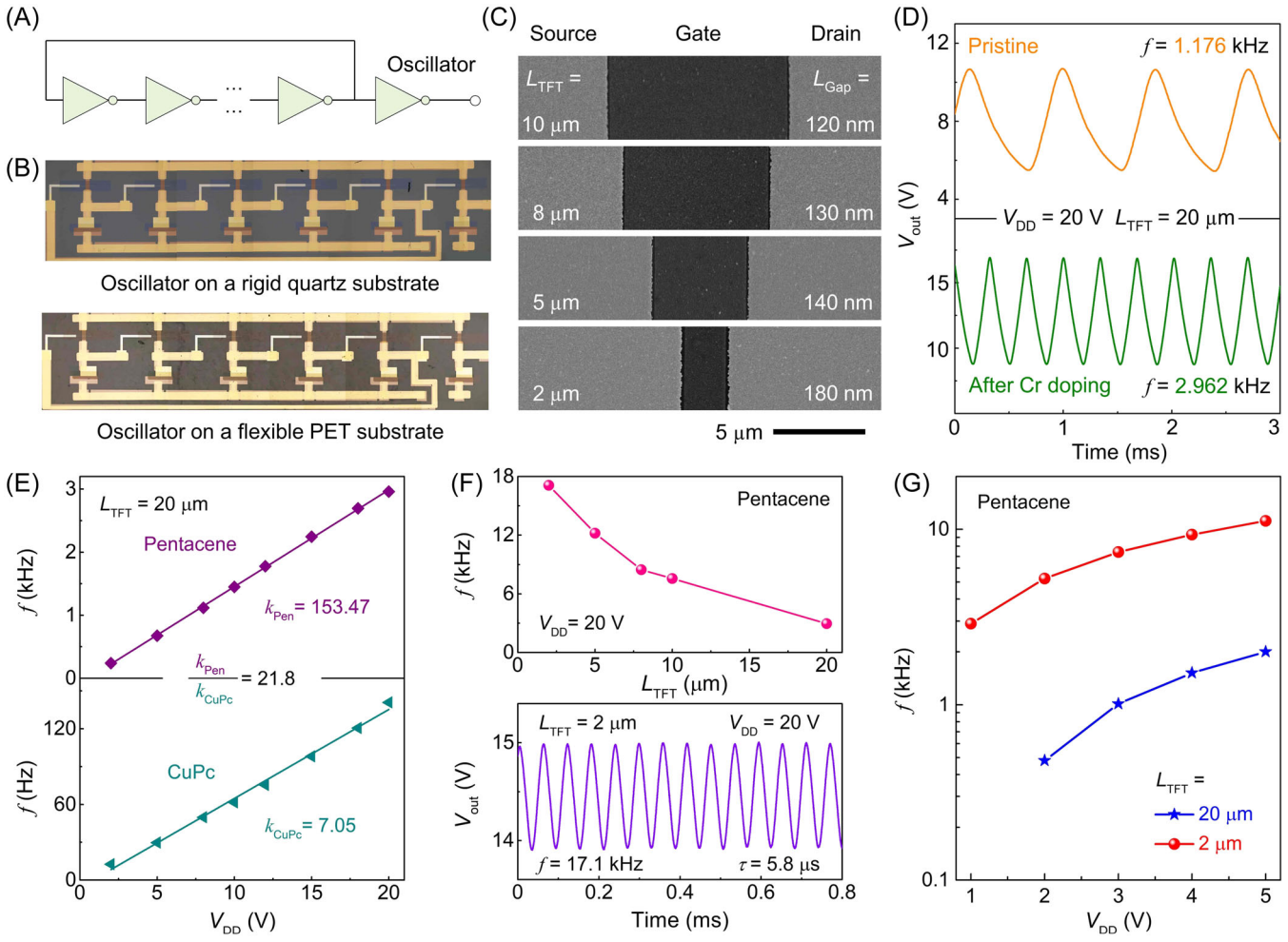

FIGURE 5 Organic ring oscillators (ROs) and their dynamic circuit characteristics. (A) Schematic illustrating the oscillator circuit. (B) Photographs showing two five-stage pentacene ROs fabricated on different substrates: a rigid quartz substrate (top) and a flexible polyethylene terephthalate (PET) substrate (bottom). The circuit occupies an area of approximately 11 mm × 2.4 mm. (C) Scanning electron microscope (SEM) images displaying the dependence of the etching degree on the organic thin-film transistor (OTFT) channel length (L_{TFT}) under identical wet-etching conditions. (D) Comparison of the output signal of two five-stage ROs based on 20-μm-long transistor channels before (top) and after (bottom) Cr doping, operating at the same driving voltage (V_{DD}) of 20 V. (E) Oscillation frequency (f) of the ROs as a function of V_{DD} for two organic semiconductors (OSCs) (top: pentacene; bottom: CuPc). (F) Top: oscillation frequency of the ROs as a function of L_{TFT}. Bottom: Measured output waveform of an RO exhibiting an f of 17.1 kHz. (G) Operating frequencies of two ROs with L_{TFT} values of 2 and 20 μm as a function of V_{DD}.

the relationship between the oscillation frequency and the Cr doping of the contact. Unsurprisingly, the zone-selective Cr doping of the contacts in the nanogaps leads to a significant increase in the working frequency. Therefore, all subsequent discussions concerning the ROs will refer to the modified devices, where the Cr layer remains within the nanogaps.

According to the well-established model of TFTs, the characteristic frequency of a transistor and the oscillation frequency of ROs should be proportional to the driving voltage and the intrinsic mobility of the semiconductor being used.[15,53] However, previous studies have shown that it is not possible to realize ROs with significantly improved f by exploiting high-mobility OSCs due to the limitations imposed by C_p.[48,51,54–56] By completely removing C_p through the d-SA method and effectively reducing the contact resistance through Cr doping (especially for devices with $L_{TFT} = 20\,\mu m$), we observed a linear relationship between f and V_{DD} in both pentacene- and CuPc-based ROs (Figure 5E). The ratio of the two slopes (153.47 Hz/V for pentacene and 7.05 Hz/V for CuPc) is consistent with the ratio of the mobilities of pentacene- and CuPc-based OTFTs with identical channel lengths (0.301 and 0.013 $cm^2/(V{\cdot}s)$, respectively). This result strongly implies that f can be increased by further optimizing the intrinsic mobility of OSCs in such C_p-free device configurations. It is worth emphasizing that the channel length also imparts significant influence on the operating frequency of organic circuits.[15] Efforts to further reduce L_{TFT} provide another promising avenue to the improvement of transit frequency.

Figure 5F summarizes the f values of these ROs based on pentacene with various L_{TFT} ranging from 2 to 20 μm. Under a V_{DD} of 20 V, the pentacene-based ROs exhibit the highest f of 17.1 kHz and a corresponding τ of 5.8 μs when utilizing OTFTs with a 2-μm-long channel. Remarkably, even when driven by a relatively low V_{DD} of 2 V, the f of such an RO based on a transistor with a 2-μm-long channel remains higher than 1.0 kHz (Supporting Information S1: Figure S20). This is a successful demonstration of the possibility of using the self-alignment technology for realizing totally C_p-free organic ROs; interestingly, the signal delays in the inverters made of C_p-free transistors and rectifying diodes are below the averages reported in previous works (Supporting Information S1: Table S3). Moreover, the ROs fabricated on PET substrates also benefit from operating at a high V_{DD} (Supporting Information S1: Figure S21). At a relatively low V_{DD} of less than 10 V, the flexible ROs oscillated at almost the same frequency as those on a rigid substrate. However, when the V_{DD} increased to above 15 V, the oscillation frequency of the ROs on the PET sheets started to lag behind, possibly due to the poor heat dissipation of plastics. Bending fatigue tests carried out at different bending radii revealed that the f of a flexible RO remained above 90% of its original level when bent around a cylinder with a radius of 6 mm (Supporting Information S1: Figure S22A). Even after 400 bending cycles with a curvature radius of 16 mm, the f dropped by less than 12%, suggesting that these devices possess superior mechanical robustness against deformation (Supporting Information S1: Figure S22B). Although the working frequencies of PMOS ROs are largely determined by the driving OTFTs, their operating voltage could be further decreased by converting the diode connection polarity in the inverter (Supporting Information S1: Figure S23). Thanks to the lower resistance of the reversely connected load diodes, the benchmark f of 10 kHz could also be achieved at a small V_{DD} of 5 V (Figure 5G) at the expense of a slightly higher power consumption (Supporting Information S1: Figure S24).

3 | CONCLUSION

In summary, we proposed a simple d-SA method to avoid any lateral overlap between the G electrode and the S/D electrodes, enabling the fabrication of organic ICs free of C_p. By tuning the wet-etching conditions, the distance from the Au contact electrodes to the semiconducting channel could be reduced to 65 nm. The spontaneously oxidized Cr layer in the nanogap further reduced the contact resistance through the doping of the hole-transporting semiconductors, namely CuPc and pentacene. This contact doping approach led to well-performing, discrete OTFTs with mobilities exceeding 0.4 $cm^2/(V{\cdot}s)$ and ON/OFF current ratios surpassing 10^5. In addition to realizing individual transistors and transistor arrays, we demonstrated the fabrication of PMOS inverters and five-stage ROs on both rigid and flexible substrates. The C_p-free ROs can not only operate at a low driving voltage of 1 V but also two different strategies reach an f in the kHz range (up to 17.1 kHz). Considering the state-of-the-art achievements in high-mobility OSCs, there is significant potential for frequency optimization of these C_p-free ROs by shortening the G-to-contact nanogaps and utilizing high-performance ambipolar semiconductors. The complete removal of C_p from these ROs, which are representative SSICs, opens up new and exciting possibilities for the realization of flexible ICs with increasingly high f in the future.

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CONFLICTS OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available in the supplementary material of this article.

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SUPPORTING INFORMATION

Additional supporting information can be found online in the Supporting Information section at the end of this article.

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